Very Large Scale Integration curriculum

EDXcellence

1ST YEAR – TRAINING

Basic Topics:

1...Introduction to VLSI:

- History and evolution of VLSI technology
- Moore's Law
- VLSI design flow
- Design methodologies: Full-custom, Semi-custom, and ASIC
- Overview of fabrication process (CMOS Technology)

2...Digital Logic Design

- Logic gates and Boolean algebra
- Combinational circuits: Adders, Multiplexers, Decoders, etc.
- Sequential circuits: Flip-flops, Latches, Counters, Registers
- State machines (Finite State Machines)
- Number systems and binary arithmetic

1ST YEAR – TRAINING

3...CMOS Technology

- CMOS transistors: NMOS and PMOS
- CMOS inverter characteristics
- Power dissipation in CMOS circuits
- Threshold voltage and body effect
- Stick diagrams and layout design rules

4...Verilog/VHDL Basics

- Introduction to Hardware Description Languages (HDLs)
- Basic syntax and structure of Verilog/VHDL
- Combinational and sequential circuit design using Verilog/VHDL
- Simulation and testing of digital designs

Intermediate Topics:-

5...CMOS Circuit Design:

- Design and analysis of CMOS combinational logic circuits
- Static and dynamic CMOS logic
- Pass-transistor logic, Transmission gates

1ST YEAR – TRAINING

- Sizing of transistors in logic gates
- Design of sequential circuits (Flip-flops, Latches)

6...Timing Analysis

- Timing parameters: Setup time, hold time, clock skew, jitter
- Static Timing Analysis (STA)
- Timing constraints and clock distribution
- Metastability and synchronization

7...Analog VLSI Design

- Basic analog components: Current mirrors, Differential pairs
- Operational amplifiers (Op-Amps)
- Analog layout considerations
- Analog-to-Digital (ADC) and Digital-to-Analog Converters (DAC)
- Phase-locked loops (PLLs) and clock generation

1ST YEAR – TRAINING

8...Memory Design

- Basics of memory cells: SRAM, DRAM
- ROM and PROM design
- Sense amplifiers and write circuits
- Memory hierarchy and cache memory
- Non-volatile memories: Flash, EEPROM

Advanced Topics:-

9...Low Power VLSI Design

- Power dissipation in CMOS circuits
- Techniques for low-power design: Clock gating, Power gating, Multi-Vt design
- Dynamic voltage and frequency scaling (DVFS)
- Sub-threshold logic design

10... Physical Design Automation

- Floor planning and partitioning
- Placement and routing algorithms
- Design rule checking (DRC) and Layout vs. Schematic (LVS) verification
- Parasitic extraction and post-layout simulation

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11...Design for Testability (DFT)

- Basics of fault models and testing
- Scan chain design and Built-In Self-Test (BIST)
- Boundary scan and JTAG
- Automatic Test Pattern Generation (ATPG)

12...ASIC Design and Verification

- ASIC design flow: From RTL to GDSII
- Functional verification and formal verification techniques
- Synthesis and optimization techniques
- Design for manufacturability (DFM) and yield considerations

1ST YEAR – TRAINING

13...Advanced FPGA Design

- FPGA architecture and configuration
- Advanced FPGA features: Embedded processors, DSP blocks, and high-speed I/O
- High-level synthesis (HLS) for FPGAs
- System-on-Chip (SoC) design using FPGAs

14...Emerging Trends in VLSI

- FinFET and beyond-CMOS devices
- 3D ICs and TSV (Through-Silicon Via) technology
- Quantum computing and quantum-dot cellular automata (QCA)
- Neuromorphic computing and VLSI for AI/ML applications

- This structured progression should provide a solid foundation in VLSI, taking you from fundamental concepts to advanced topics.

2ND YEAR - PROJECTS

PROJECTS:-

- Basic circuits written ni Verilog HDL, simulated and implemented on the FPGA Digital Design
- VART communication to print a single character
- FSM Designs-Mealy &Moore Machines and Up Down Counter This curriculum can be adapted based on the learner's pace and specific requirements

3RD YEAR – INTERNSHIPS

- **Guaranteed internship opportunity to gain practical exposure.**

Task: - Working on the internship Project.

Improved Lead Scoring with FPGA Technology Accelerating Lead Processing

- Real-time Insights: FPGAs can significantly speed up the computation of lead scores, allowing salesteams to immediately prioritize and engage with the most promising prospects.
- Handling Large Datasets With their parallel processing capabilities, FPGAs can handle massive amounts of lead data, ensuring that no opportunity is missed.

4TH YEAR – PLACEMENT

- Automated resume
- aptitude training
- mock exams
- mock interviews
- career counselling
- continuous support

- This roadmap should provide a solid foundation in VLSI , covering the essential topics and preparing you for more advanced studies or real-world applications.